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UNIVERSITAT POLITÈCNICA DE CATALUNYA

Anexos

"DESARROLLO DE UNA UNIDAD DE CONTROL ELECTRÓNICO (ECU) DEDICADA AL GOBIERNO DE MOTORES DE COMBUSTIÓN INTERNA"

PFC presentado para optar al título de Ingeniero Técnico Industrial especialidad ELECTRÓNICA

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CÓDIGO DEL PROGRAMA

Microcontrolador 1

```
#include <18F4550.h>
#device adc=10
#fuses NOWDT,HS, NOPUT, NOPROTECT
#use delay(clock=20000000)
#use fast_io(B)
#include <lcd4x20.c>
/**********************DECLARACION DE VARIABLES*******************************/

Int16 TEP=0,RPM6;
float avf;
Int cont=0;


int16 q,a,i,rev,revol,av,temp,t;
int16 iny[10][10]={{2240,3600,4800,5240,5700,5770,5790,5030,5760,5790}
                   {2230,3601,4801,5241,5701,5771,5791,5031,5761,5791}
                   {2000,3602,4802,5242,5702,5772,5792,5032,5762,5792}
                   {2000,3603,4803,5243,5703,5773,5793,5033,5763,5793}
                   {2000,2980,4620,5070,5740,5850,5980,5990,6050,6040}
                   {2000,2460,3880,4400,5110,5260,5380,5410,5640,5400}
                   {2000,3220,4490,4960,5500,5600,5650,5160,5720,5660}
                   {2000,2400,3950,4560,5560,5850,6030,5890,6110,6110}
                   {2000,2400,3790,4690,6040,6580,6720,6360,6720,6720}
                   {2000,2300,3050,4510,5550,5980,6000,6050,6060,6020}};

int16 avc[10][10]={{200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {400,562,403,359,348,334,330,328,328,329}
                   {400,560,527,517,448,421,404,373,372,374}
                   {600,600,580,555,549,500,485,503,490,492}
                   {600,600,534,493,440,459,464,464,459,462}
                   {600,600,479,457,431,416,416,419,416,415}
                   {600,600,488,491,471,470,442,455,452,451}};

/************************************INTERRUPCIONES*****************************/
#int_ext
void funcion_ext_int(){
  TEP=get_timer1();         //Valor del Timer1
  set_timer1(0);            //Inicializa TMR1
```

```
  cont++;
  if(cont==1){

    output_high(PIN_B5);      //Señal de inyeccion
    output_low(PIN_B5);
  }
  if(cont==10){
    output_high(PIN_B4);      //Pulso para calcular revoluciones en PIC2
    output_low(PIN_B4);
  }
  if(cont==11){
    output_high(PIN_B4);      //Pulso para calcular revoluciones en PIC2
    output_low(PIN_B4);
  }
  if(cont==12){
    cont=0;
  }

}


/**********************************MAIN*************************************/
void main() {

  set_tris_B(0x0F);         // B0-B3 como entrada, B4-B7 como salida
  port_b_pullups(TRUE);     //Pull-up para RB0


  setup_timer_1(T1_INTERNAL|T1_DIV_BY_4);   // ConfiguraciÛn TIMER1
  enable_interrupts(int_ext);           //Configuracion interrupciones
  ext_int_edge(0,L_TO_H);
  enable_interrupts(global);

  setup_adc(AN0_TO_AN4);            //Canal 0-4 analÛgico
  setup_adc(ADC_CLOCK_DIV_16);
  set_timer1(0);                    //Inicializa TMR1


  lcd_init();                   //Inicializa LCD


  for(;;){

  set_adc_channel(0);           //Habilitación canal0
    delay_us(5);
    q = read_adc();               //Lectura canal0
    a = q/10;



    set_adc_channel(1);           //Habilitación canal1
    delay_us(5);
    t = read_adc();               //Lectura canal1
    temp = t/10;

   If(a>100){
    a=100;
```

```
}


RPM6=500000/(2*TEP);
rev=RPM6*12.4616;


revol=rev/1000;

if ((a>=0)&(a<=10)){
   switch(revol){
       case 0: i=iny[0][0]; break;
       case 1: i=iny[1][0]; break;
       case 2: i=iny[2][0]; break;
       case 3: i=iny[3][0]; break;
       case 4: i=iny[4][0]; break;
       case 5: i=iny[5][0]; break;
       case 6: i=iny[6][0]; break;
       case 7: i=iny[7][0]; break;
       case 8: i=iny[8][0]; break;
       default: i=iny[9][0];
    }
  }
 else if((a>11)&(a<=20)){
   switch(revol){
       case 0: i=iny[0][1]; break;
       case 1: i=iny[1][1]; break;
       case 2: i=iny[2][1]; break;
       case 3: i=iny[3][1]; break;
       case 4: i=iny[4][1]; break;
       case 5: i=iny[5][1]; break;
       case 6: i=iny[6][1]; break;
       case 7: i=iny[7][1]; break;
       case 8: i=iny[8][1]; break;
       default: i=iny[9][1];
 }
 }
 else if((a>20)&(a<=30)){
    switch(revol){
       case 0: i=iny[0][2]; break;
       case 1: i=iny[1][2]; break;
       case 2: i=iny[2][2]; break;
       case 3: i=iny[3][2]; break;
       case 4: i=iny[4][2]; break;
       case 5: i=iny[5][2]; break;
       case 6: i=iny[6][2]; break;
       case 7: i=iny[7][2]; break;
       case 8: i=iny[8][2]; break;
       default: i=iny[9][2];
 }
 }
 else if((a>30)&(a<=40)){
    switch(revol){
       case 0: i=iny[0][3]; break;
       case 1: i=iny[1][3]; break;
       case 2: i=iny[2][3]; break;
       case 3: i=iny[3][3]; break;
```

```
      case 4: i=iny[4][3]; break;
      case 5: i=iny[5][3]; break;
      case 6: i=iny[6][3]; break;
      case 7: i=iny[7][3]; break;
      case 8: i=iny[8][3]; break;
      default: i=iny[9][3];
}
}
else if((a>40)&(a<=50)){
   switch(revol){
      case 0: i=iny[0][4]; break;
      case 1: i=iny[1][4]; break;
      case 2: i=iny[2][4]; break;
      case 3: i=iny[3][4]; break;
      case 4: i=iny[4][4]; break;
      case 5: i=iny[5][4]; break;
      case 6: i=iny[6][4]; break;
      case 7: i=iny[7][4]; break;
      case 8: i=iny[8][4]; break;
      default:  i=iny[9][4];
}
}
else if((a>50)&(a<=60)){
   switch(revol){
      case 0: i=iny[0][5]; break;
      case 1: i=iny[1][5]; break;
      case 2: i=iny[2][5]; break;
      case 3: i=iny[3][5]; break;
      case 4: i=iny[4][5]; break;
      case 5: i=iny[5][5]; break;
      case 6: i=iny[6][5]; break;
      case 7: i=iny[7][5]; break;
      case 8: i=iny[8][5]; break;
      default: i=iny[9][5];
}
}
else if((a>60)&(a<=70)){
   switch(revol){
      case 0: i=iny[0][6]; break;
      case 1: i=iny[1][6]; break;
      case 2: i=iny[2][6]; break;
      case 3: i=iny[3][6]; break;
      case 4: i=iny[4][6]; break;
      case 5: i=iny[5][6]; break;
      case 6: i=iny[6][6]; break;
      case 7: i=iny[7][6]; break;
      case 8: i=iny[8][6]; break;
      default: i=iny[9][6];
}
}
else if((a>70)&(a<=80)){
   switch(revol){
      case 0: i=iny[0][7]; break;
      case 1: i=iny[1][7]; break;
      case 2: i=iny[2][7]; break;
      case 3: i=iny[3][7]; break;
      case 4: i=iny[4][7]; break;
```

```
        case 5: i=iny[5][7]; break;
        case 6: i=iny[6][7]; break;
        case 7: i=iny[7][7]; break;
        case 8: i=iny[8][7]; break;
        default: i=iny[9][7];
 }
 }
 else if((a>80)&(a<=90)){
    switch(revol){
        case 0: i=iny[0][8]; break;
        case 1: i=iny[1][8]; break;
        case 2: i=iny[2][8]; break;
        case 3: i=iny[3][8]; break;
        case 4: i=iny[4][8]; break;
        case 5: i=iny[5][8]; break;
        case 6: i=iny[6][8]; break;
        case 7: i=iny[7][8]; break;
        case 8: i=iny[8][8];break;
        default: i=iny[9][8];
 }
 }
 else if(a>90){
    switch(revol){
        case 0: i=iny[0][9]; break;
        case 1: i=iny[1][9]; break;
        case 2: i=iny[2][9]; break;
        case 3: i=iny[3][9]; break;
        case 4: i=iny[4][9]; break;
        case 5: i=iny[5][9]; break;
        case 6: i=iny[6][9]; break;
        case 7: i=iny[7][9]; break;
        case 8: i=iny[8][9]; break;
        default: i=iny[9][9];
 }
 }


if ((a>=0)&(a<=10)){
   switch(revol){
        case 0: av=avc[0][0]; break;
        case 1: av=avc[1][0]; break;
        case 2: av=avc[2][0]; break;
        case 3: av=avc[3][0]; break;
        case 4: av=avc[4][0]; break;
        case 5: av=avc[5][0]; break;
        case 6: av=avc[6][0]; break;
        case 7: av=avc[7][0]; break;
        case 8: av=avc[8][0]; break;
        default: av=avc[9][0];
 }
  }
 else if((a>11)&(a<=20)){
   switch(revol){
        case 0: av=avc[0][1]; break;
        case 1: av=avc[1][1]; break;
        case 2: av=avc[2][1]; break;
        case 3: av=avc[3][1]; break;
```

```
      case 4: av=avc[4][1]; break;
      case 5: av=avc[5][1]; break;
      case 6: av=avc[6][1]; break;
      case 7: av=avc[7][1]; break;
      case 8: av=avc[8][1]; break;
      default: av=avc[9][1];
}
}
else if((a>20)&(a<=30)){
   switch(revol){
      case 0: av=avc[0][2]; break;
      case 1: av=avc[1][2]; break;
      case 2: av=avc[2][2]; break;
      case 3: av=avc[3][2]; break;
      case 4: av=avc[4][2]; break;
      case 5: av=avc[5][2]; break;
      case 6: av=avc[6][2]; break;
      case 7: av=avc[7][2]; break;
      case 8: av=avc[8][2]; break;
      default: av=avc[9][2];
}
}
else if((a>30)&(a<=40)){
   switch(revol){
      case 0: av=avc[0][3]; break;
      case 1: av=avc[1][3]; break;
      case 2: av=avc[2][3]; break;
      case 3: av=avc[3][3]; break;
      case 4: av=avc[4][3]; break;
      case 5: av=avc[5][3]; break;
      case 6: av=avc[6][3]; break;
      case 7: av=avc[7][3]; break;
      case 8: av=avc[8][3]; break;
      default: av=avc[9][3];
}
}
else if((a>40)&(a<=50)){
   switch(revol){
      case 0: av=avc[0][4]; break;
      case 1: av=avc[1][4]; break;
      case 2: av=avc[2][4]; break;
      case 3: av=avc[3][4]; break;
      case 4: av=avc[4][4]; break;
      case 5: av=avc[5][4]; break;
      case 6: av=avc[6][4]; break;
      case 7: av=avc[7][4]; break;
      case 8: av=avc[8][4]; break;
      default: av=avc[9][4];
}
}
else if((a>50)&(a<=60)){
   switch(revol){
      case 0: av=avc[0][5]; break;
      case 1: av=avc[1][5]; break;
      case 2: av=avc[2][5]; break;
      case 3: av=avc[3][5]; break;
      case 4: av=avc[4][5]; break;
```

```
      case 5: av=avc[5][5]; break;
      case 6: av=avc[6][5]; break;
      case 7: av=avc[7][5]; break;
      case 8: av=avc[8][5]; break;
      default: av=avc[9][5];
}
}
else if((a>60)&(a<=70)){
   switch(revol){
      case 0: av=avc[0][6]; break;
      case 1: av=avc[1][6]; break;
      case 2: av=avc[2][6]; break;
      case 3: av=avc[3][6]; break;
      case 4: av=avc[4][6]; break;
      case 5: av=avc[5][6]; break;
      case 6: av=avc[6][6]; break;
      case 7: av=avc[7][6]; break;
      case 8: av=avc[8][6]; break;
      default: av=avc[9][6];
}
}
else if((a>70)&(a<=80)){
   switch(revol){
      case 0: av=avc[0][7]; break;
      case 1: av=avc[1][7]; break;
      case 2: av=avc[2][7]; break;
      case 3: av=avc[3][7]; break;
      case 4: av=avc[4][7]; break;
      case 5: av=avc[5][7]; break;
      case 6: av=avc[6][7]; break;
      case 7: av=avc[7][7]; break;
      case 8: av=avc[8][7]; break;
      default: av=avc[9][7];
}
}
else if((a>80)&(a<=90)){
   switch(revol){
      case 0: av=avc[0][8]; break;
      case 1: av=avc[1][8]; break;
      case 2: av=avc[2][8]; break;
      case 3: av=avc[3][8]; break;
      case 4: av=avc[4][8]; break;
      case 5: av=avc[5][8]; break;
      case 6: av=avc[6][8]; break;
      case 7: av=avc[7][8]; break;
      case 8: av=avc[8][8]; break;
      default: av=avc[9][8];
}
}
else if(a>90){
   switch(revol){
      case 0: av=avc[0][9]; break;
      case 1: av=avc[1][9]; break;
      case 2: av=avc[2][9]; break;
      case 3: av=avc[3][9]; break;
      case 4: av=avc[4][9]; break;
      case 5: av=avc[5][9]; break;
```

```
        case 6: av=avc[6][9]; break;
        case 7: av=avc[7][9]; break;
        case 8: av=avc[8][9]; break;
        default: av=avc[9][9];
    }
    }



if(temp<=60){
   i=i*1.1;
}


if(rev>10000){
   i=0;
}

avf=av/10.0;

lcd_gotoxy(1,1);
printf(lcd_putc, "A=%3lu ", a);
lcd_gotoxy(10,1);
printf(lcd_putc, "Tp=%3lu C", temp);
lcd_gotoxy(1,2);
printf(lcd_putc, "Rev =%5lu rpm", rev);
lcd_gotoxy(1,3);
printf(lcd_putc, "Tin=%5lu us", i);
lcd_gotoxy(1,4);
printf(lcd_putc, "Avan=%3.1f g", avf);


}
}
```

Microcontrolador 2

```
#include <18F4550.h>
#device adc=10
#fuses NOWDT,HS, NOPUT, NOPROTECT,USBDIV,PLL5,VREGEN,NOLVP,NODEBUG
#device high_ints=TRUE
#use delay(clock=20000000)

#define USB_HID_DEVICE     FALSE
#define USB_EP1_TX_ENABLE  USB_ENABLE_BULK
#define USB_EP1_RX_ENABLE  USB_ENABLE_BULK
#define USB_EP1_TX_SIZE    64
#define USB_EP1_RX_SIZE    64

#include <pic18_usb.h>
#include <PicUSB.h>        //Configuracion del USB y los descriptores para este dispositivo
#include <usb.c>




/*****************************DECLARACION DE VARIABLES*************************************/

float aux,aux1,aux2,aux3,aux4,aux5,bujia,av1,mch,trev;
int cont=0;
int8 a,temp;
int8  iH,iL,revH,revL,avH,avL;
lnt16 TEP=0,RPM6,tin,av,tbuj,t;
int16 q,i,rev,revol;
int8 envio[8];
int16 iny[10][10]={{2240,3600,4800,5240,5700,5770,5790,5030,5760,5790}
                   {2230,3601,4801,5241,5701,5771,5791,5031,5761,5791}
                   {2000,3602,4802,5242,5702,5772,5792,5032,5762,5792}
                   {2000,3603,4803,5243,5703,5773,5793,5033,5763,5793}
                   {2000,2980,4620,5070,5740,5850,5980,5990,6050,6040}
                   {2000,2460,3880,4400,5110,5260,5380,5410,5640,5400}
                   {2000,3220,4490,4960,5500,5600,5650,5160,5720,5660}
                   {2000,2400,3950,4560,5560,5850,6030,5890,6110,6110}
                   {2000,2400,3790,4690,6040,6580,6720,6360,6720,6720}
                   {2000,2300,3050,4510,5550,5980,6000,6050,6060,6020}};

int16 avc[10][10]={{200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {200,300,300,300,300,300,300,300,300,300}
                   {400,562,403,359,348,334,330,328,328,329}
                   {400,560,527,517,448,421,404,373,372,374}
                   {600,600,580,555,549,500,485,503,490,492}
                   {600,600,534,493,440,459,464,464,459,462}
                   {600,600,479,457,431,416,416,419,416,415}
                   {600,600,488,491,471,470,442,455,452,451}};
```

```
/*****************************INTERRUPCIONES*****************************************************/

#int_ext1                          //interrupcion calculo rpm
void funcion_ext_int1(){

  if(cont==0){
    TEP=get_timer1();
    cont++;
  }
  if(cont==1){
    set_timer1(0);

    cont=0;
  }

}


#int_ext high                      //Interrupcion inicio de inyeccion
void funcion_ext_int(){                //carga de timers
  output_high(PIN_B5);
  output_high(PIN_B4);
  set_timer0(tin);
  set_timer1(tbuj);
  cont=0;

 }

#int_timer0                        //Interrupcion de apagado inyeccion
void funcion_int_timer0(){

  output_low(PIN_B4);

}

#int_timer1                        //interrupcion de encendido
void funcion_int_timer1(){

  output_low(PIN_B5);

}

/************************************MAIN*********************************************************/
void main() {

  set_tris_B(0x0F);                // B0-B3 como entrada, B4-B7 como salida
  port_b_pullups(TRUE);              //Pull-up para RB0


  setup_timer_1(T1_INTERNAL|T1_DIV_BY_4);
  setup_timer_0(RTCC_INTERNAL|RTCC_DIV_8);
  enable_interrupts(int_ext);              //Habilitacion interrupciones
  enable_interrupts(int_ext1);
  enable_interrupts(int_timer0);
  enable_interrupts(int_timer1);
  ext_int_edge(0,L_TO_H);
  enable_interrupts(global);
```

```
  setup_adc(AN0_TO_AN4);              //Canal 0-4 analogico
  setup_adc(ADC_CLOCK_DIV_16);        //Reloj del ADC entre 16


usb_init();
usb_wait_for_enumeration();

for (;;) {


  set_adc_channel(0);           //Habilitacion canal0
    delay_us(5);
    q = read_adc();               //Lectura canal0
    a = q/10;

  set_adc_channel(1);           //Habilitacion canal1
    delay_us(5);
    t = read_adc();               //Lectura canal1
    temp = t/10;

  If(a>100){
    a=100;
   }


  RPM6=500000/(2*TEP);
  rev=RPM6*12.4616;

  revol=rev/1000;

   if ((a>=0)&(a<=10)){
     switch(revol){
         case 0: i=iny[0][0]; break;
         case 1: i=iny[1][0]; break;
         case 2: i=iny[2][0]; break;
         case 3: i=iny[3][0]; break;
         case 4: i=iny[4][0]; break;
         case 5: i=iny[5][0]; break;
         case 6: i=iny[6][0]; break;
         case 7: i=iny[7][0]; break;
         case 8: i=iny[8][0]; break;
         default: i=iny[9][0];
      }
     }
    else if((a>11)&(a<=20)){
      switch(revol){
         case 0: i=iny[0][1]; break;
         case 1: i=iny[1][1]; break;
         case 2: i=iny[2][1]; break;
         case 3: i=iny[3][1]; break;
         case 4: i=iny[4][1]; break;
         case 5: i=iny[5][1]; break;
         case 6: i=iny[6][1]; break;
         case 7: i=iny[7][1]; break;
         case 8: i=iny[8][1]; break;
         default: i=iny[9][1];
```

```
}
}
else if((a>20)&(a<=30)){
   switch(revol){
      case 0: i=iny[0][2]; break;
      case 1: i=iny[1][2]; break;
      case 2: i=iny[2][2]; break;
      case 3: i=iny[3][2]; break;
      case 4: i=iny[4][2]; break;
      case 5: i=iny[5][2]; break;
      case 6: i=iny[6][2]; break;
      case 7: i=iny[7][2]; break;
      case 8: i=iny[8][2]; break;
      default: i=iny[9][2];
}
}
else if((a>30)&(a<=40)){
   switch(revol){
      case 0: i=iny[0][3]; break;
      case 1: i=iny[1][3]; break;
      case 2: i=iny[2][3]; break;
      case 3: i=iny[3][3]; break;
      case 4: i=iny[4][3]; break;
      case 5: i=iny[5][3]; break;
      case 6: i=iny[6][3]; break;
      case 7: i=iny[7][3]; break;
      case 8: i=iny[8][3]; break;
      default: i=iny[9][3];
}
}
else if((a>40)&(a<=50)){
   switch(revol){
      case 0: i=iny[0][4]; break;
      case 1: i=iny[1][4]; break;
      case 2: i=iny[2][4]; break;
      case 3: i=iny[3][4]; break;
      case 4: i=iny[4][4]; break;
      case 5: i=iny[5][4]; break;
      case 6: i=iny[6][4]; break;
      case 7: i=iny[7][4]; break;
      case 8: i=iny[8][4]; break;
      default:  i=iny[9][4];
}
}
else if((a>50)&(a<=60)){
   switch(revol){
      case 0: i=iny[0][5]; break;
      case 1: i=iny[1][5]; break;
      case 2: i=iny[2][5]; break;
      case 3: i=iny[3][5]; break;
      case 4: i=iny[4][5]; break;
      case 5: i=iny[5][5]; break;
      case 6: i=iny[6][5]; break;
      case 7: i=iny[7][5]; break;
      case 8: i=iny[8][5]; break;
      default: i=iny[9][5];
}
```

```
}
else if((a>60)&(a<=70)){
   switch(revol){
      case 0: i=iny[0][6]; break;
      case 1: i=iny[1][6]; break;
      case 2: i=iny[2][6]; break;
      case 3: i=iny[3][6]; break;
      case 4: i=iny[4][6]; break;
      case 5: i=iny[5][6]; break;
      case 6: i=iny[6][6]; break;
      case 7: i=iny[7][6]; break;
      case 8: i=iny[8][6]; break;
      default: i=iny[9][6];
}
}
else if((a>70)&(a<=80)){
   switch(revol){
      case 0: i=iny[0][7]; break;
      case 1: i=iny[1][7]; break;
      case 2: i=iny[2][7]; break;
      case 3: i=iny[3][7]; break;
      case 4: i=iny[4][7]; break;
      case 5: i=iny[5][7]; break;
      case 6: i=iny[6][7]; break;
      case 7: i=iny[7][7]; break;
      case 8: i=iny[8][7]; break;
      default: i=iny[9][7];
}
}
else if((a>80)&(a<=90)){
   switch(revol){
      case 0: i=iny[0][8]; break;
      case 1: i=iny[1][8]; break;
      case 2: i=iny[2][8]; break;
      case 3: i=iny[3][8]; break;
      case 4: i=iny[4][8]; break;
      case 5: i=iny[5][8]; break;
      case 6: i=iny[6][8]; break;
      case 7: i=iny[7][8]; break;
      case 8: i=iny[8][8];break;
      default: i=iny[9][8];
}
}
else if(a>90){
   switch(revol){
      case 0: i=iny[0][9]; break;
      case 1: i=iny[1][9]; break;
      case 2: i=iny[2][9]; break;
      case 3: i=iny[3][9]; break;
      case 4: i=iny[4][9]; break;
      case 5: i=iny[5][9]; break;
      case 6: i=iny[6][9]; break;
      case 7: i=iny[7][9]; break;
      case 8: i=iny[8][9]; break;
      default: i=iny[9][9];
}
}
```

```
if ((a>=0)&(a<=10)){
        switch(revol){
            case 0: av=avc[0][0]; break;
            case 1: av=avc[1][0]; break;
            case 2: av=avc[2][0]; break;
            case 3: av=avc[3][0]; break;
            case 4: av=avc[4][0]; break;
            case 5: av=avc[5][0]; break;
            case 6: av=avc[6][0]; break;
            case 7: av=avc[7][0]; break;
            case 8: av=avc[8][0]; break;
            default: av=avc[9][0];
      }
       }
      else if((a>11)&(a<=20)){
        switch(revol){
            case 0: av=avc[0][1]; break;
            case 1: av=avc[1][1]; break;
            case 2: av=avc[2][1]; break;
            case 3: av=avc[3][1]; break;
            case 4: av=avc[4][1]; break;
            case 5: av=avc[5][1]; break;
            case 6: av=avc[6][1]; break;
            case 7: av=avc[7][1]; break;
            case 8: av=avc[8][1]; break;
            default: av=avc[9][1];
      }
      }
      else if((a>20)&(a<=30)){
         switch(revol){
            case 0: av=avc[0][2]; break;
            case 1: av=avc[1][2]; break;
            case 2: av=avc[2][2]; break;
            case 3: av=avc[3][2]; break;
            case 4: av=avc[4][2]; break;
            case 5: av=avc[5][2]; break;
            case 6: av=avc[6][2]; break;
            case 7: av=avc[7][2]; break;
            case 8: av=avc[8][2]; break;
            default: av=avc[9][2];
      }
      }
      else if((a>30)&(a<=40)){
         switch(revol){
            case 0: av=avc[0][3]; break;
            case 1: av=avc[1][3]; break;
            case 2: av=avc[2][3]; break;
            case 3: av=avc[3][3]; break;
            case 4: av=avc[4][3]; break;
            case 5: av=avc[5][3]; break;
            case 6: av=avc[6][3]; break;
            case 7: av=avc[7][3]; break;
            case 8: av=avc[8][3]; break;
            default: av=avc[9][3];
      }
      }
      else if((a>40)&(a<=50)){
```

```
   switch(revol){
      case 0: av=avc[0][4]; break;
      case 1: av=avc[1][4]; break;
      case 2: av=avc[2][4]; break;
      case 3: av=avc[3][4]; break;
      case 4: av=avc[4][4]; break;
      case 5: av=avc[5][4]; break;
      case 6: av=avc[6][4]; break;
      case 7: av=avc[7][4]; break;
      case 8: av=avc[8][4]; break;
      default: av=avc[9][4];
}
}
else if((a>50)&(a<=60)){
   switch(revol){
      case 0: av=avc[0][5]; break;
      case 1: av=avc[1][5]; break;
      case 2: av=avc[2][5]; break;
      case 3: av=avc[3][5]; break;
      case 4: av=avc[4][5]; break;
      case 5: av=avc[5][5]; break;
      case 6: av=avc[6][5]; break;
      case 7: av=avc[7][5]; break;
      case 8: av=avc[8][5]; break;
      default: av=avc[9][5];
}
}
else if((a>60)&(a<=70)){
   switch(revol){
      case 0: av=avc[0][6]; break;
      case 1: av=avc[1][6]; break;
      case 2: av=avc[2][6]; break;
      case 3: av=avc[3][6]; break;
      case 4: av=avc[4][6]; break;
      case 5: av=avc[5][6]; break;
      case 6: av=avc[6][6]; break;
      case 7: av=avc[7][6]; break;
      case 8: av=avc[8][6]; break;
      default: av=avc[9][6];
}
}
else if((a>70)&(a<=80)){
   switch(revol){
      case 0: av=avc[0][7]; break;
      case 1: av=avc[1][7]; break;
      case 2: av=avc[2][7]; break;
      case 3: av=avc[3][7]; break;
      case 4: av=avc[4][7]; break;
      case 5: av=avc[5][7]; break;
      case 6: av=avc[6][7]; break;
      case 7: av=avc[7][7]; break;
      case 8: av=avc[8][7]; break;
      default: av=avc[9][7];
}
}
else if((a>80)&(a<=90)){
   switch(revol){
```

```
            case 0: av=avc[0][8]; break;
            case 1: av=avc[1][8]; break;
            case 2: av=avc[2][8]; break;
            case 3: av=avc[3][8]; break;
            case 4: av=avc[4][8]; break;
            case 5: av=avc[5][8]; break;
            case 6: av=avc[6][8]; break;
            case 7: av=avc[7][8]; break;
            case 8: av=avc[8][8]; break;
            default: av=avc[9][8];
      }
      }
      else if(a>90){
         switch(revol){
            case 0: av=avc[0][9]; break;
            case 1: av=avc[1][9]; break;
            case 2: av=avc[2][9]; break;
            case 3: av=avc[3][9]; break;
            case 4: av=avc[4][9]; break;
            case 5: av=avc[5][9]; break;
            case 6: av=avc[6][9]; break;
            case 7: av=avc[7][9]; break;
            case 8: av=avc[8][9]; break;
            default: av=avc[9][9];
      }
      }

    if(temp<=60){
      i=i*1.1;
   }
    if(rev>10000){
      i=0;
   }

/*******************************CALCULO DEL AVANCE EN TIEMPO*******************************/
    trev=60000000/rev;
    av1=av/10.0;
    mch=(trev/360)*av1;
    bujia=trev-mch;


/*******************************CARGA TIMER 1, ENCENDIDO***********************************/
    aux3=bujia*0.2463;
    aux4=aux3/1000000.000000000000;
    aux5=1250000.000000000000*aux4;
    tbuj=65536-aux5;


/*******************************CARGA TIMER 0, INYECCIO************************************/
   aux=i*0.25;
   aux1=aux/1000000.000000000000;
   aux2=625000.000000000000*aux1;
   tin=65536-aux2;


iL=make8(i,0); //LSB
iH=make8(i,1); //MSB
```

```
revL=make8(rev,0); //LSB
revH=make8(rev,1); //MSB
avL=make8(av,0); //LSB
avH=make8(av,1); //MSB

envio[0]=a;
envio[1]=temp;
envio[2]=iH;
envio[3]=iL;
envio[4]=revH;
envio[5]=revL;
envio[6]=avH;
envio[7]=avL;

   usb_task();
   if(usb_enumerated()){

   usb_put_packet(1,envio,8,USB_DTS_TOGGLE);


      }

  }
}
```

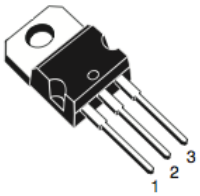
DATOS
TÉCNICOS

- TIP112

TIP110/112
TIP115/117

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

- STMicroelectronics PREFERRED SALESTYPES
- COMPLEMENTARY PNP - NPN DEVICES
- MONOLITHIC DARLINGTON CONFIGURATION
- INTEGRATED ANTIPARALLEL COLLECTOR-EMITTER DIODE



TO-220

APPLICATIONS

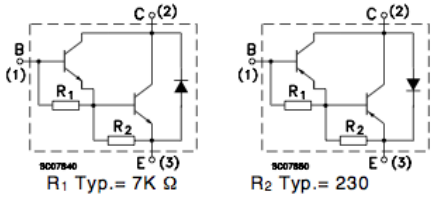
- LINEAR AND SWITCHING INDUSTRIAL EQUIPMENT

DESCRIPTION

The TIP110 and TIP112 are silicon Epitaxial-Base NPN transistors in monolithic Darlington configuration mounted in Jedec TO-220 plastic package. They are intented for use in medium power linear and switching applications.

The complementary PNP types are TIP115 and TIP117.

INTERNAL SCHEMATIC DIAGRAM



R_1 Typ.= 7K Ω R_2 Typ.= 230

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value		Unit
		NPN	TIP110	TIP112	
		PNP	TIP115	TIP117	
V_{CBO}	Collector-Base Voltage (I_E = 0)		60	100	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)		60	100	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)		5		V
I_C	Collector Current		2		A
I_{CM}	Collector Peak Current		4		A
I_B	Base Current		50		mA
P_{tot}	Total Dissipation at $T_{case} \leq 25$ °C $T_{amb} \leq 25$ °C		50 2		W W
T_{stg}	Storage Temperature		-65 to 150		°C
T_j	Max. Operating Junction Temperature		150		°C

* For PNP types voltage and current values are negative

THERMAL DATA

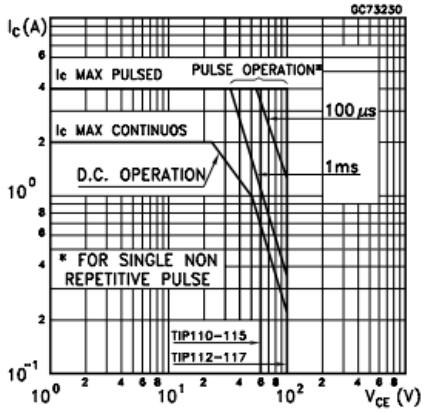
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	2.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

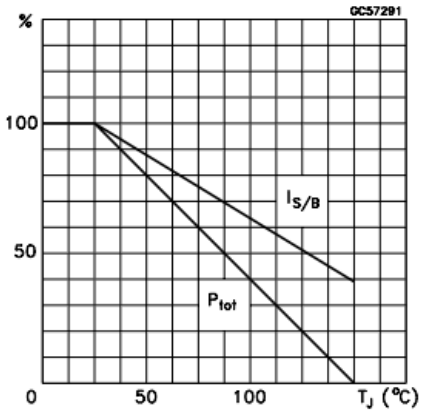
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = Half Rated V_{CEO}			2	mA
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CB} = Rated V_{CBO}			1	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			2	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 30 mA for **TIP110/115** for **TIP112/117**	 60 100			 V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 2 A I_B = 8 mA			2.5	V
V_{BE}*	Base-Emitter Voltage	I_C = 2 A V_{CE} = 4 V			2.8	V
h_{FE}*	DC Current Gain	I_C = 1 A V_{CE} = 4 V I_C = 2 A V_{CE} = 4 V	1000 500			

* Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %
For PNP types voltage and current values are negative.

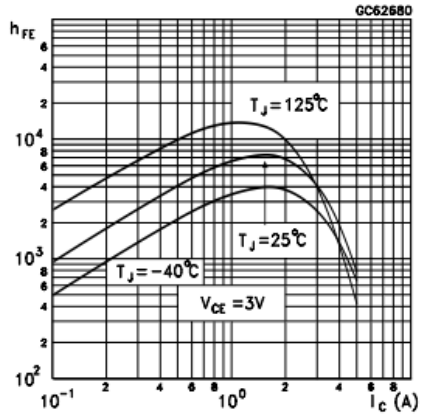
Safe Operating Areas



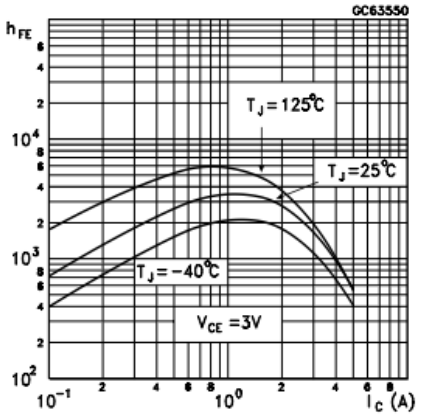
Derating Curve



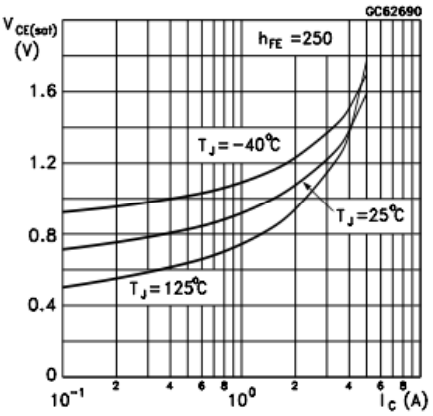
DC Current Gain (NPN type)



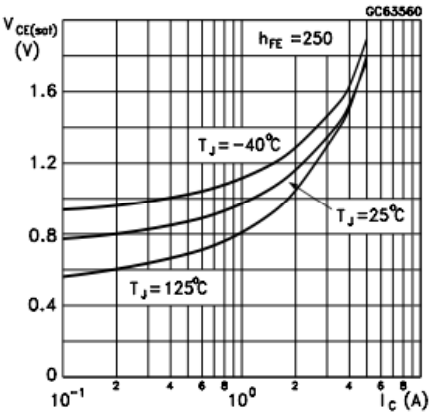
DC Current Gain (PNP type)



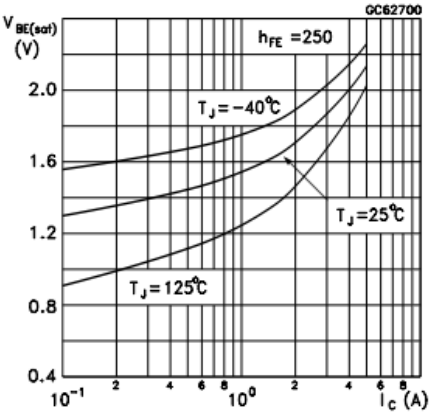
Collector-Emitter Saturation Voltage (NPN type)



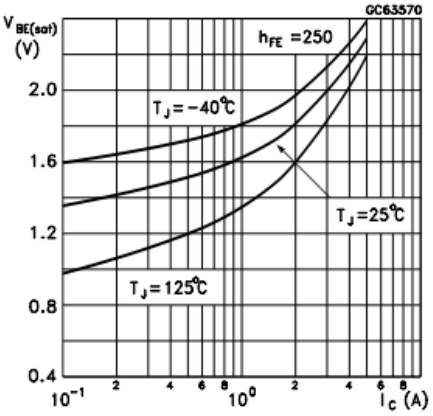
Collector-Emitter Saturation Voltage (PNP type)



Base-Emitter Saturation Voltage (NPN type)



Base-Emitter Saturation Voltage (PNP type)



- 12N60A4

FAIRCHILD SEMICONDUCTOR®

HGTP12N60A4, HGTG12N60A4, HGT1S12N60A4S9A

Data Sheet **August 2003**

600V, SMPS Series N-Channel IGBTs

The HGTP12N60A4, HGTG12N60A4 and HGT1S12N60A4S9A are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

This IGBT is ideal for many high voltage switching applications operating at high frequencies where low conduction losses are essential. This device has been optimized for high frequency switch mode power supplies.

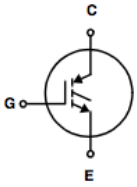
Formerly Developmental Type TA49335.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60A4	TO-220AB	12N60A4
HGTG12N60A4	TO-247	12N60A4
HGT1S12N60A4S9A	TO-263AB	12N60A4

NOTE: When ordering, use the entire part number.

Symbol



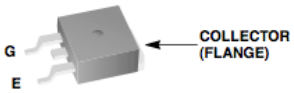
Features

- >100kHz Operation at 390V, 12A
- 200kHz Operation at 390V, 9A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . 70ns at T_J = 125°C
- Low Conduction Loss
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards

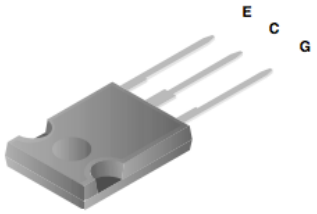
Packaging

JEDEC TO-220AB ALTERNATE VERSION

JEDEC TO-263AB



JEDEC STYLE TO-247



FAIRCHILD CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG12N60A4, HGTP12N60A4, HGT1S12N60A4S9A	UNITS
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	54	A
At $T_C = 110^oC$	I_{C110}	23	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 2	SSOA	60A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	167	W
Power Dissipation Derating $T_C > 25^oC$		1.33	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Lead Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Tech Brief 334	T_{PKG}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. Pulse width limited by maximum junction temperature.

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	$I_C = -10mA$, $V_{GE} = 0V$		20	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = 600V$	$T_J = 25^oC$	-	-	250	μA
			$T_J = 125^oC$	-	-	2.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 12A$, $V_{GE} = 15V$	$T_J = 25^oC$	-	2.0	2.7	V
			$T_J = 125^oC$	-	1.6	2.0	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = 600V$		-	5.6	-	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$, $L = 100\mu H$, $V_{CE} = 600V$		60	-	-	A
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = 12A$, $V_{CE} = 300V$		-	8	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = 12A$, $V_{CE} = 300V$	$V_{GE} = 15V$	-	78	96	nC
			$V_{GE} = 20V$	-	97	120	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 25^oC$, $I_{CE} = 12A$, $V_{CE} = 390V$, $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 500\mu H$, Test Circuit (Figure 20)		-	17	-	ns
Current Rise Time	t_{rI}			-	8	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	96	-	ns
Current Fall Time	t_{fI}			-	18	-	ns
Turn-On Energy (Note 3)	E_{ON1}			-	55	-	μJ
Turn-On Energy (Note 3)	E_{ON2}			-	160	-	μJ
Turn-Off Energy (Note 2)	E_{OFF}			-	50	-	μJ

Electrical Specifications $T_J = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	IGBT and Diode at $T_J = 125^oC$	-	17	-	ns
Current Rise Time	t_{rI}	$I_{CE} = 12A$	-	16	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$	$V_{CE} = 390V$	-	110	170	ns
Current Fall Time	t_{fI}	$V_{GE} = 15V$	-	70	95	ns
Turn-On Energy (Note 3)	E_{ON1}	$R_G = 10\Omega$	-	55	-	μJ
Turn-On Energy (Note 3)	E_{ON2}	$L = 500\mu H$	-	250	350	μJ
Turn-Off Energy (Note 2)	E_{OFF}	Test Circuit (Figure 20)	-	175	285	μJ
Thermal Resistance Junction To Case	$R_{\theta JC}$		-	-	0.75	$^oC/W$

NOTES:

2. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.
3. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in Figure 20.

Typical Performance Curves Unless Otherwise Specified

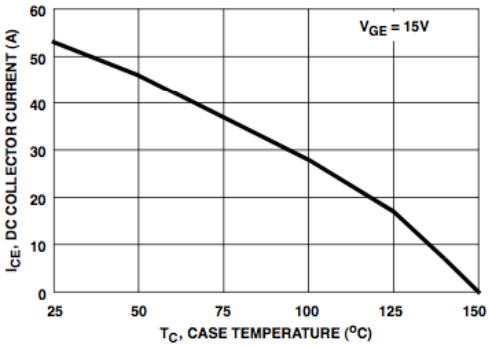


FIGURE 1. DC COLLECTOR CURRENT vs CASE TEMPERATURE

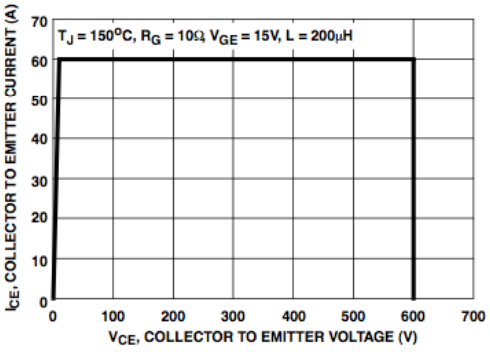


FIGURE 2. MINIMUM SWITCHING SAFE OPERATING AREA

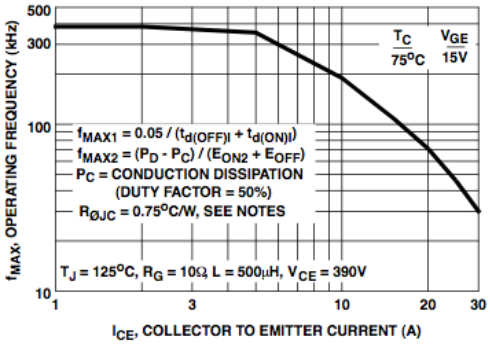


FIGURE 3. OPERATING FREQUENCY vs COLLECTOR TO EMITTER CURRENT

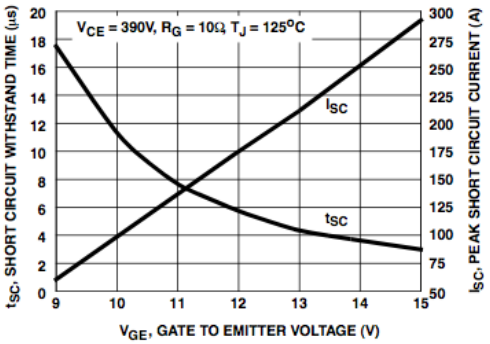


FIGURE 4. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves Unless Otherwise Specified (Continued)

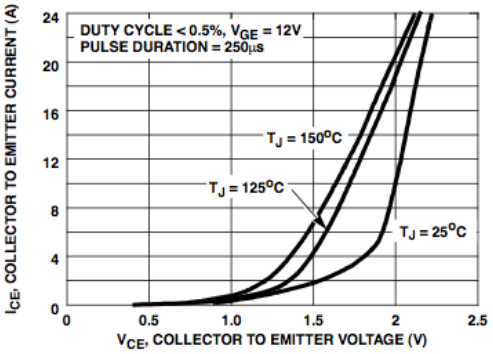


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

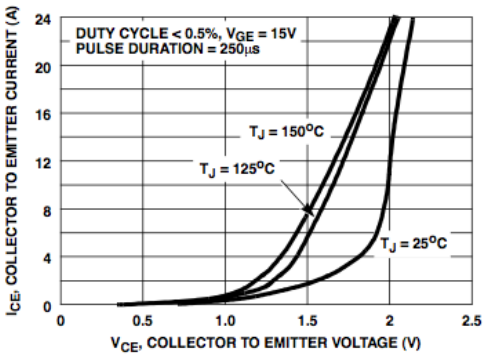


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

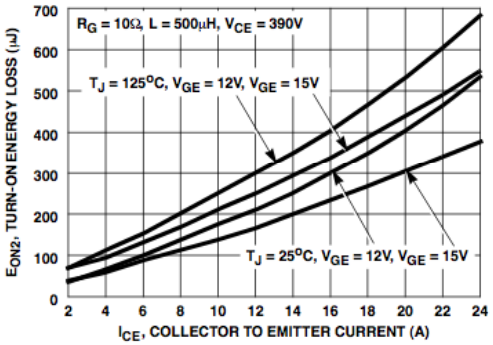


FIGURE 7. TURN-ON ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

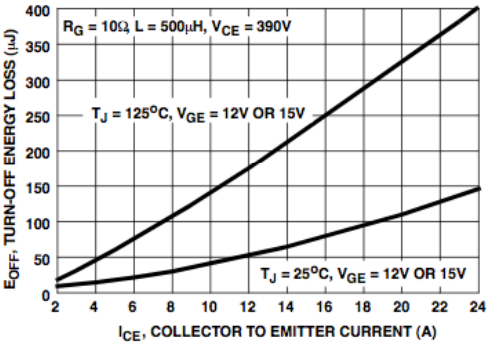


FIGURE 8. TURN-OFF ENERGY LOSS vs COLLECTOR TO EMITTER CURRENT

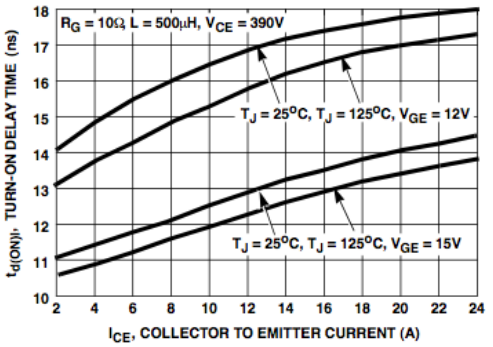


FIGURE 9. TURN-ON DELAY TIME vs COLLECTOR TO EMITTER CURRENT

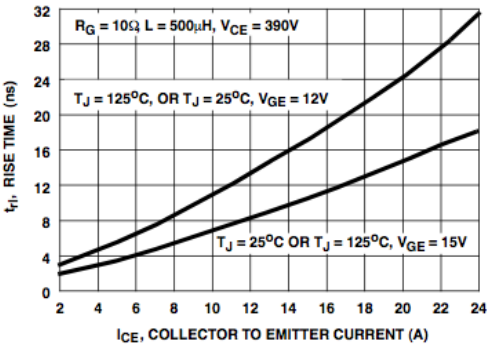


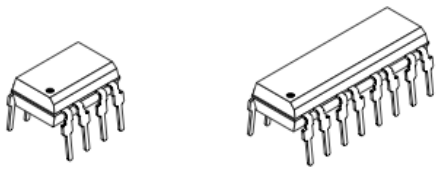
FIGURE 10. TURN-ON RISE TIME vs COLLECTOR TO EMITTER CURRENT

- CNY74-2H

Multichannel Optocoupler with Phototransistor Output

Description

The CNY74-2H and CNY74-4H consist of a phototransistor optically coupled to a gallium arsenide infrared-emitting diode in an 8-lead, resp. 16-lead plastic dual inline package.
The elements are mounted on one leadframe using a **coplanar technique**, providing a fixed distance between input and output for highest safety requirements.



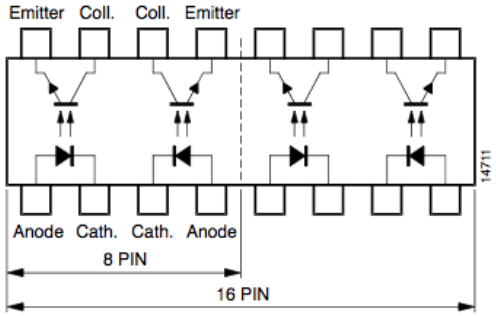
14926

Applications

Galvanically separated circuits, non-interacting switches

Features

- CNY74-2H includes 2 isolater channels
- CNY74-4H includes 4 isolater channels
- Isolation test voltage V_{IO} = 5 kV
- Test class 25/100/21 DIN 40 045
- Low coupling capacitance of typical 0.3 pF
- **C**urrent **T**ransfer **R**atio (CTR) of typical 100%
- Low temperature coefficient of CTR
- Wide ambient temperature range
- **U**nderwriters **L**aboratory (UL) 1577 recognized, file number E-76222
- **CSA** (C–UL) 1577 recognized, file number E-76222 – Double Protection
- Coupling System U



Order Instruction

Ordering Code	CTR Ranking	Remarks
CNY74–2H	50 to 600%	8 Pin = Dual channel
CNY74–4H	50 to 600%	16 Pin = Quad channel

Absolute Maximum Ratings

Input (Emitter)

Parameter	Test Conditions	Symbol	Value	Unit
Reverse voltage		V_R	6	V
Forward current		I_F	60	mA
Forward surge current	$t_p \le 10\mu s$	I_{FSM}	1.5	A
Power dissipation	$T_{amb} \le 25°C$	P_V	100	mW
Junction temperature		T_j	125	°C

Output (Detector)

Parameter	Test Conditions	Symbol	Value	Unit
Collector emitter voltage		V_{CEO}	70	V
Emitter collector voltage		V_{ECO}	7	V
Collector current		I_C	50	mA
Peak collector current	$t_p/T = 0.5$, $t_p \le 10$ ms	I_{CM}	100	mA
Power dissipation	$T_{amb} \le 25°C$	P_V	150	mW
Junction temperature		T_j	125	°C

Coupler

Parameter	Test Conditions	Symbol	Value	Unit
AC isolation test voltage (RMS)	t = 1 min	V_{IO} [1]	5	kV
Total power dissipation	$T_{amb} \le 25°C$	P_{tot}	250	mW
Ambient temperature range		T_{amb}	–40 to +100	°C
Storage temperature range		T_{stg}	–55 to +125	°C
Soldering temperature	2 mm from case, t ≤ 10 s	T_{sd}	260	°C

[1] Related to standard climate 23/50 DIN 50014

Electrical Characteristics (T_{amb} = 25°C)

Input (Emitter)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Forward voltage	I_F = 50 mA	V_F		1.25	1.6	V

Output (Detector)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Collector emitter voltage	I_C = 1 mA	V_{CEO}	70			V
Emitter collector voltage	I_E = 100 µA	V_{ECO}	7			V
Collector dark current	V_{CE} = 20 V, I_F = 0, E = 0	I_{CEO}			100	nA

Coupler

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
DC isolation test voltage	t = 2 s	V_{IO} [1)]	5			kV
Isolation resistance	V_{IO} = 1000 V, 40% relative humidity	R_{IO} [1)]		10^{12}		Ω
Collector emitter saturation voltage	I_F = 10 mA, I_C = 1 mA	V_{CEsat}			0.3	V
Cut-off frequency	V_{CE} = 5 V, I_F = 10 mA, R_L = 100 Ω	f_c		100		kHz
Coupling capacitance	f = 1 MHz	C_k		0.3		pF
[1)] Related to standard climate 23/50 DIN 50014						

Current Transfer Ratio (CTR)

Parameter	Test Conditions	Type	Symbol	Min.	Typ.	Max.	Unit
I_C/I_F	V_{CE} = 5 V, I_F = 5 mA		CTR	0.5	1.0	6.0	
	V_{CE} = 5 V, I_F = 10 mA		CTR	0.6	1.2		

Switching Characteristics

Parameter	Test Conditions	Symbol	Typ.	Unit
Delay time	V_S = 5 V, I_C = 2 mA, R_L = 100 Ω (see figure 1)	t_d	3.0	µs
Rise time		t_r	3.0	µs
Fall time		t_f	4.7	µs
Storage time		t_s	0.3	µs
Turn-on time		t_{on}	6.0	µs
Turn-off time		t_{off}	5.0	µs
Turn-on time	V_S = 5 V, I_F = 10 mA, R_L = 1 kΩ (see figure 2)	t_{on}	9.0	µs
Turn-off time		t_{off}	18.0	µs

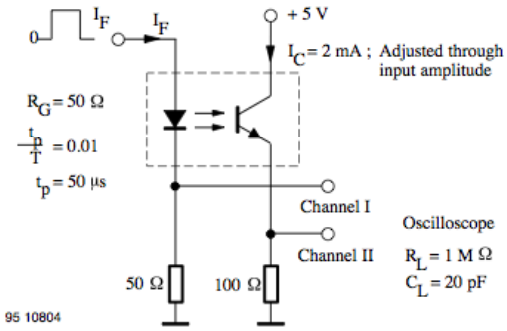


Figure 1. Test circuit, non-saturated operation

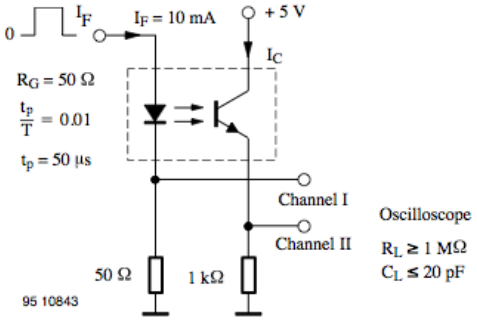
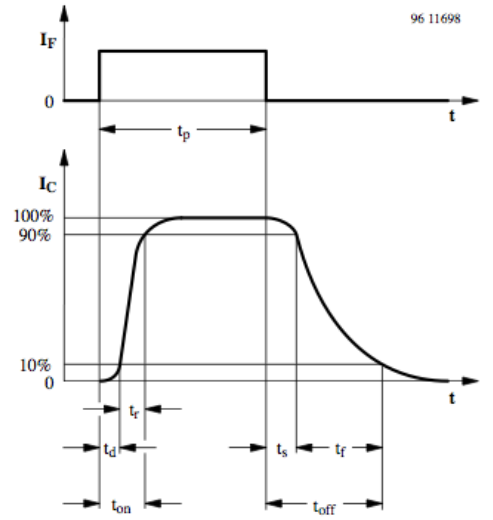


Figure 2. Test circuit, saturated operation



t_p	pulse duration	t_s	storage time
t_d	delay time	t_f	fall time
t_r	rise time	t_{off} (= t_s + t_f)	turn-off time
t_{on} (= t_d + t_r)	turn-on time		

Figure 3. Switching times

Typical Characteristics (T_{amb} = 25°C, unless otherwise specified)

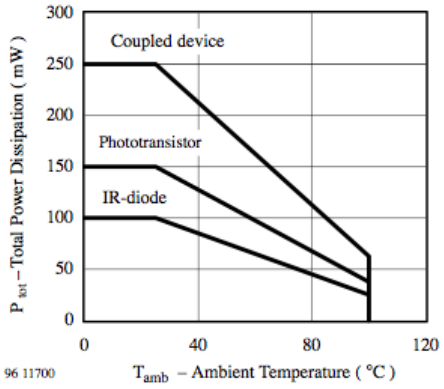


Figure 4. Total Power Dissipation vs. Ambient Temperature

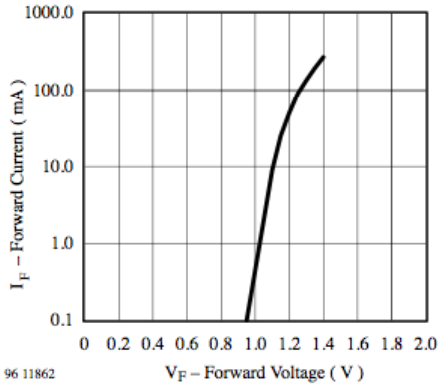


Figure 5. Forward Current vs. Forward Voltage

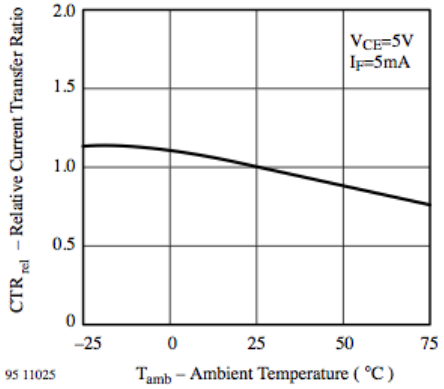


Figure 6. Relative Current Transfer Ratio vs. Ambient Temperature

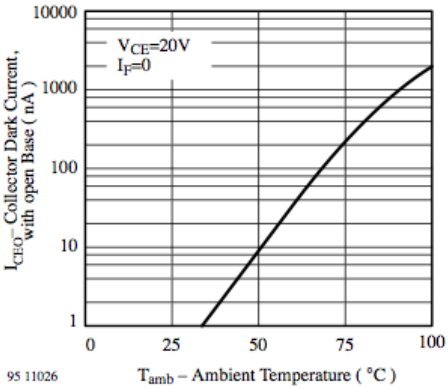


Figure 7. Collector Dark Current vs. Ambient Temperature

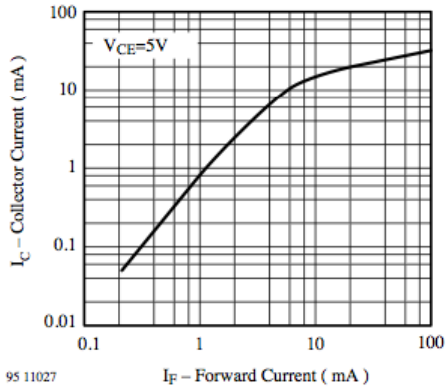


Figure 8. Collector Current vs. Forward Current

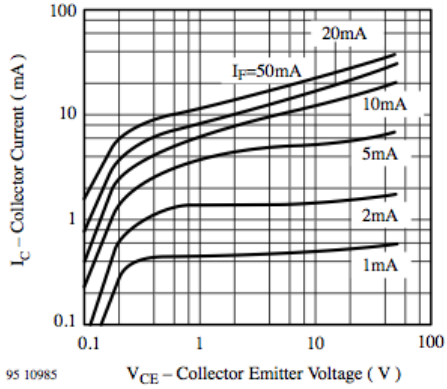


Figure 9. Collector Current vs. Collector Emitter Voltage

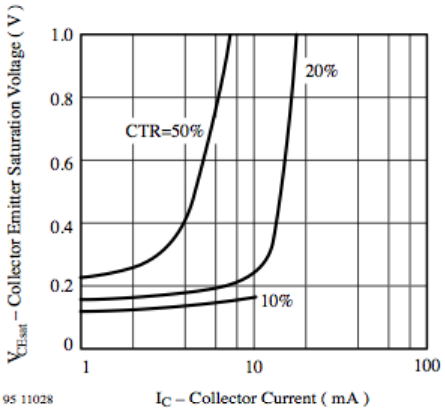


Figure 10. Collector Emitter Saturation Voltage vs. Collector Current

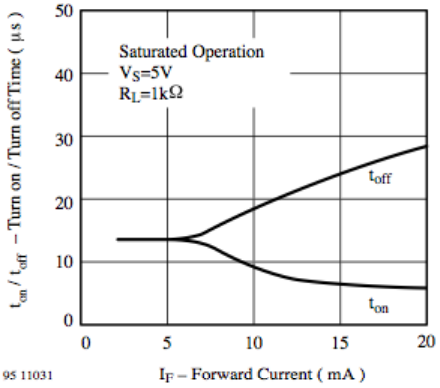


Figure 12. Turn on / off Time vs. Forward Current

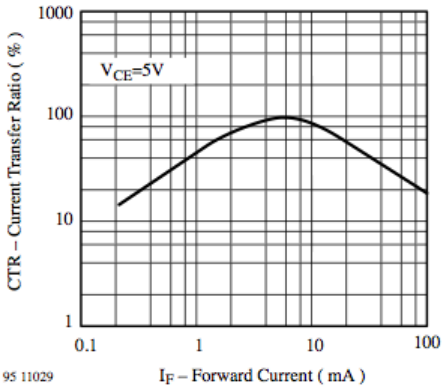


Figure 11. Current Transfer Ratio vs. Forward Current

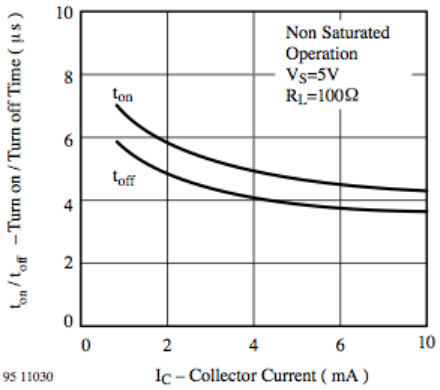


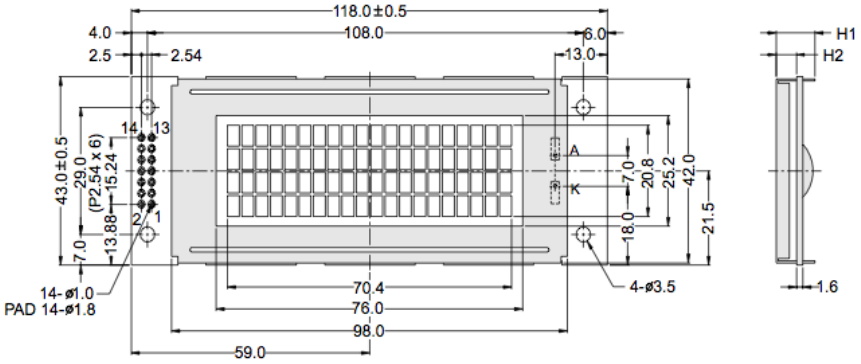
Figure 13. Turn on / off Time vs. Collector Current

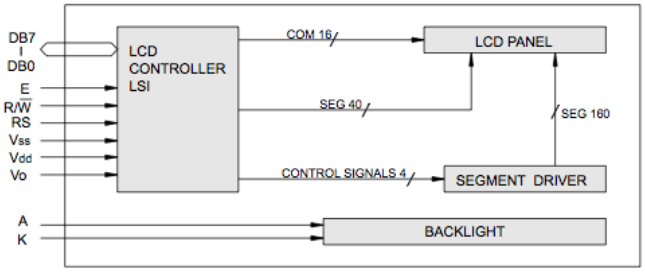
- PC 2004

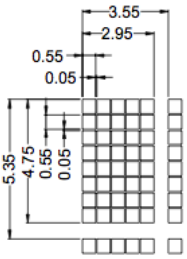
POWERTIP

PC 2004-B

OUTLINE DIMENSION & BLOCK DIAGRAM







The tolerance unless classified ± 0.3mm

MECHANICAL SPECIFICATION			
Overall Size	118.0 x 43.0	Module	H2 / H1
View Area	76.0 x 25.2	W /O B/L	5.0 / 9.6
Dot Size	0.55 x 0.55	EL B/L	5.0 / 9.6
Dot Pitch	0.60 x 0.60	LED B/L	8.7 / 13.3

PIN ASSIGNMENT		
Pin no.	Symbol	Function
1	Vss	Power supply(GND)
2	Vdd	Power supply(+)
3	Vo	Contrast Adjust
4	RS	Register select signal
5	R/W	Data read / write
6	E	Enable signal
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line

ABSOLUTE MAXIMUM RATING					
Item	Symbol	Condition	Min.	Max.	Units
Supply for logic voltage	Vdd-Vss	25°C	-0.3	7	V
LCD driving supply voltage	Vdd-Vee	25°C	-0.3	13	V
Input voltage	Vin	25°C	-0.3	Vdd+0.3	V

ELECTRICAL CHARACTERISTICS											
Item	Symbol	Condition	Min.		Typical		Max.		Units
Power supply voltage	Vdd-Vss	25°C	2.7		–		5.5		V
LCD operation voltage	Vop	Top	N	W	N	W	N	W	V
		-20°C	–	7.1	–	7.5	–	7.9	V
		0°C	5.3	–	5.7	–	6.1	–	V
		25°C	5	6.1	5.4	6.4	5.8	6.7	V
		50°C	4.7	–	5.1	–	5.5	–	V
		70°C	–	5.7	–	6	–	6.3	V
LCM current consumption (No B/L)	Idd	Vdd=5V	–		2.5		4		mA
Backlight current consumption	LED/edge	VB/L=4.2V	–		–		–		mA
	LED/array	VB/L=4.2V	–		260		–		mA

- PIC 18F4550

MICROCHIP **PIC18F2455/2550/4455/4550**

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1 Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 5.8 μA Typical
- Sleep mode Currents Down to 0.1 μA Typical
- Timer1 Oscillator: 1.1 μA Typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μA Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High-Precision PLL for USB
- Two External Clock modes, Up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator Options allow Microcontroller and USB module to Run at Different Clock Speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-Bit, Up to 13-Channel Analog-to-Digital Converter (A/D) module with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

Special Microcontroller Features:

- C Compiler Optimized Architecture with Optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: > 40 Years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Optional Dedicated ICD/ICSP Port (44-pin, TQFP package only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

40-Pin PDIP

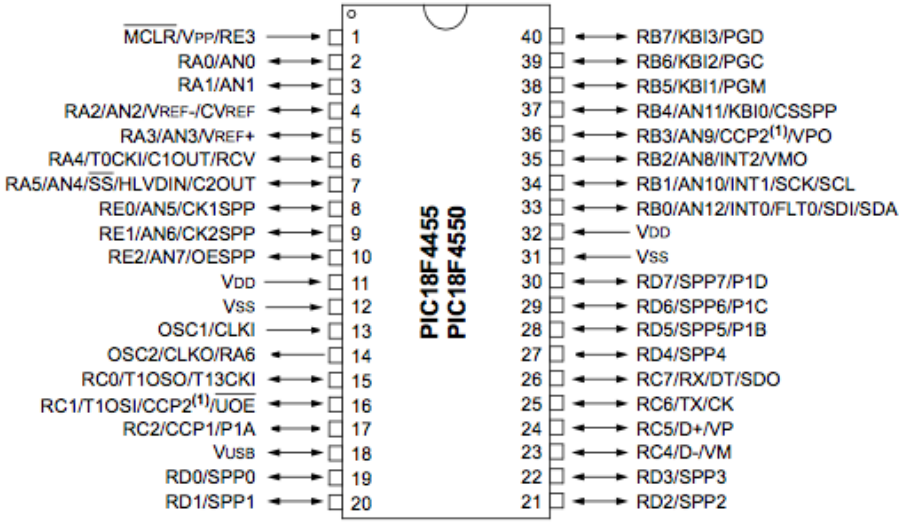
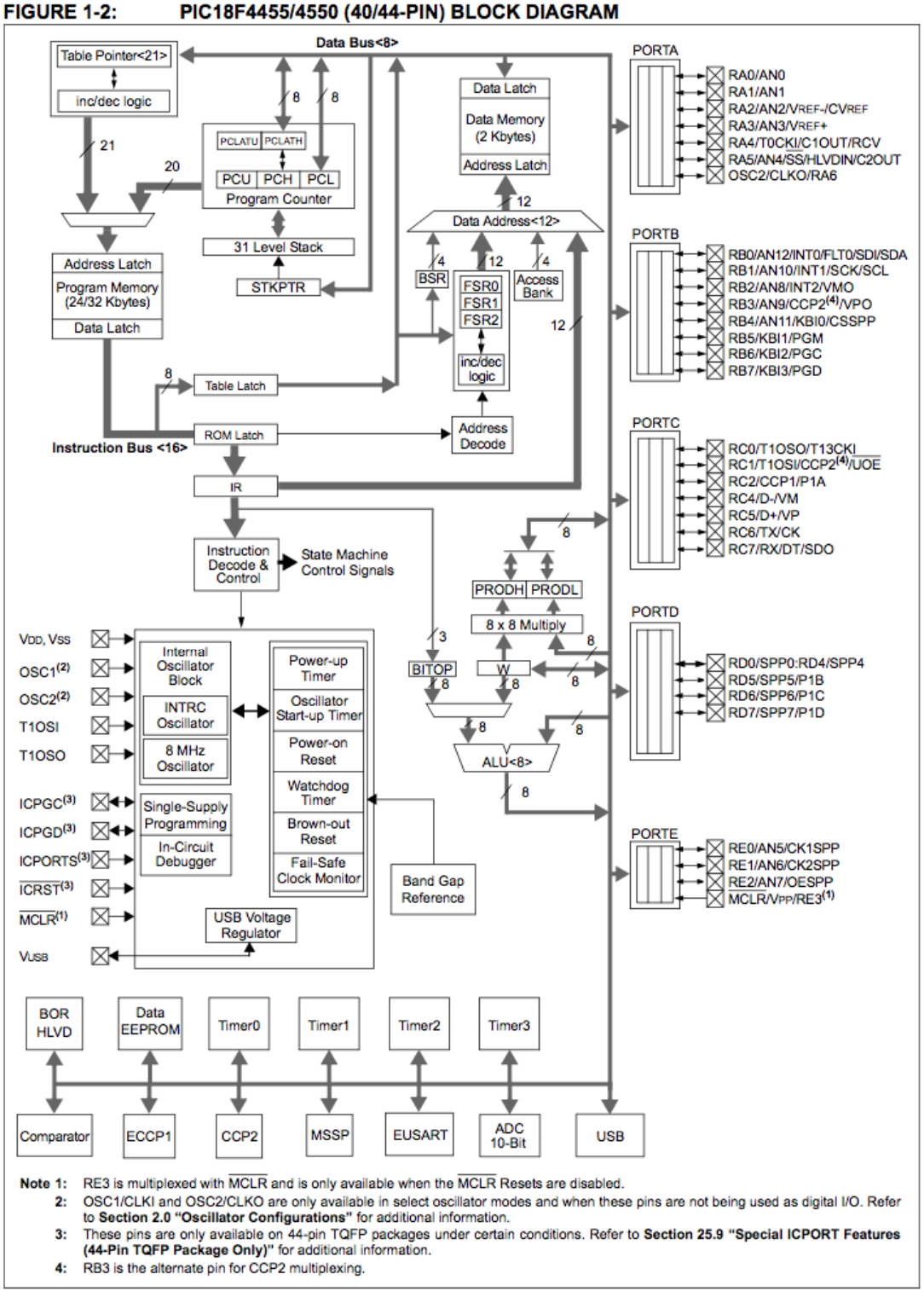


TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-Pin PDIP 28-Pin SOIC	28-Pin PDIP 28-Pin SOIC	40-Pin PDIP 44-Pin QFN 44-Pin TQFP	40-Pin PDIP 44-Pin QFN 44-Pin TQFP

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with $\overline{\text{MCLR}}$ and is only available when the $\overline{\text{MCLR}}$ Resets are disabled.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to **Section 25.9 "Special ICPORT Features (44-Pin TQFP Package Only)"** for additional information.

4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3	1	18	18			Master Clear (input) or programming voltage (input).
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/SS/HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
SS				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog input 12.
INT0				I	ST	External interrupt 0.
FLT0				I	ST	Enhanced PWM Fault input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog input 10.
INT1				I	ST	External interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog input 8.
INT2				I	ST	External interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/$\overline{UOE}$	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
$\overline{UOE}$				O	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/AN5/CK1SPP	8	25	25			
RE0				I/O	ST	Digital I/O.
AN5				I	Analog	Analog input 5.
CK1SPP				O	—	SPP clock 1 output.
RE1/AN6/CK2SPP	9	26	26			
RE1				I/O	ST	Digital I/O.
AN6				I	Analog	Analog input 6.
CK2SPP				O	—	SPP clock 2 output.
RE2/AN7/OESPP	10	27	27			
RE2				I/O	ST	Digital I/O.
AN7				I	Analog	Analog input 7.
OESPP				O	—	SPP output enable output.
RE3	—	—	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	P	—	Internal USB 3.3V voltage regulator output, positive supply for the USB transceiver.
NC/ICCK/ICPGC(3)	—	—	12			No Connect or dedicated ICD/ICSP™ port clock.
ICCK				I/O	ST	In-Circuit Debugger clock.
ICPGC				I/O	ST	ICSP programming clock.
NC/ICDT/ICPGD(3)	—	—	13			No Connect or dedicated ICD/ICSP port clock.
ICDT				I/O	ST	In-Circuit Debugger data.
ICPGD				I/O	ST	ICSP programming data.
NC/$\overline{ICRST}$/ICVPP(3)	—	—	33			No Connect or dedicated ICD/ICSP port Reset.
$\overline{ICRST}$				I	—	Master Clear (Reset) input.
ICVPP				P	—	Programming voltage input.
NC/ICPORTS(3)	—	—	34	P	—	No Connect or 28-pin device emulation.
ICPORTS						Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

2.2 Oscillator Types

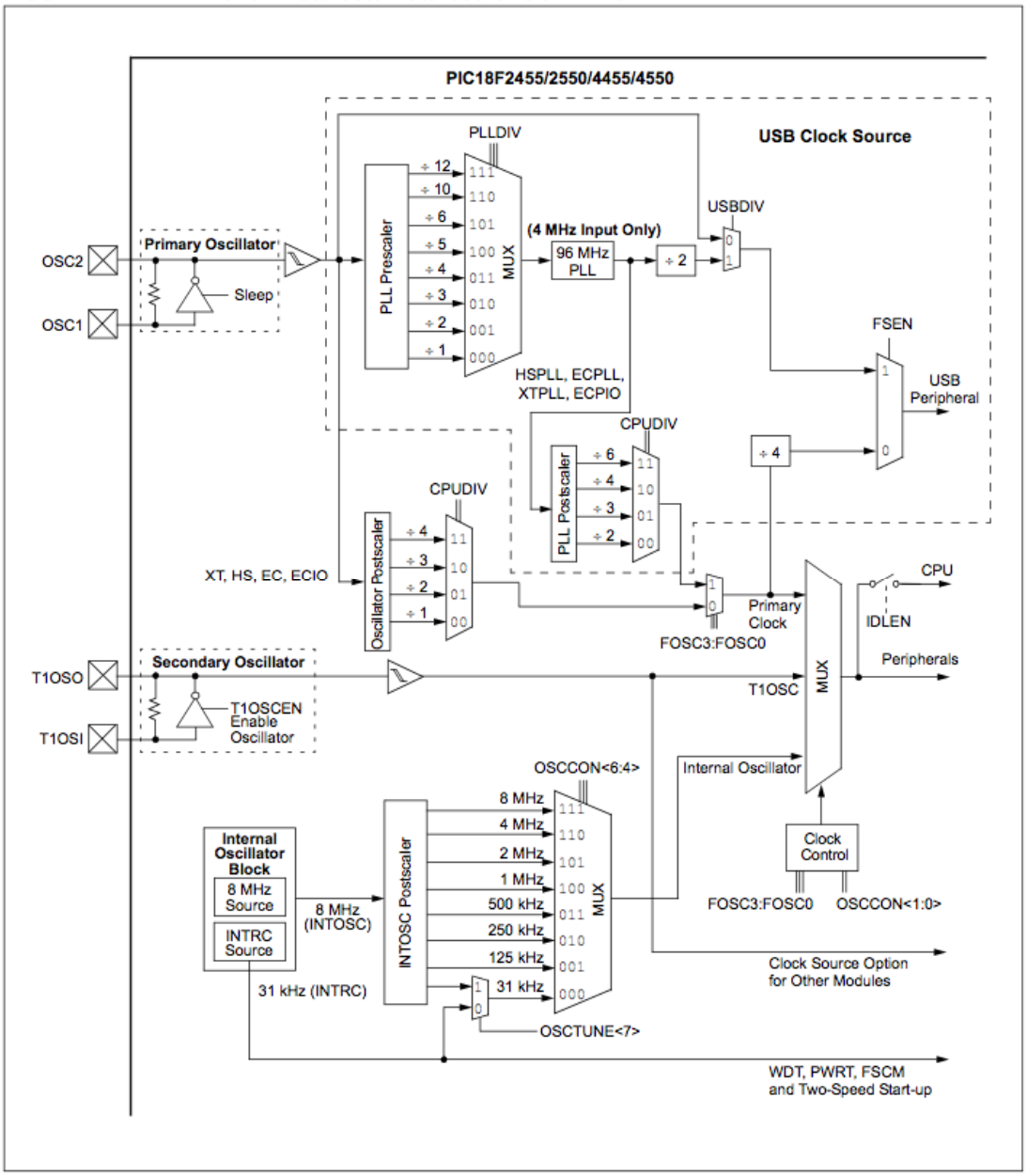
PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

1. XT Crystal/Resonator
2. HS High-Speed Crystal/Resonator
3. HSPLL High-Speed Crystal/Resonator with PLL Enabled
4. EC External Clock with FOSC/4 Output
5. ECIO External Clock with I/O on RA6
6. ECPLL External Clock with PLL Enabled and FOSC/4 Output on RA6
7. ECPIO External Clock with PLL Enabled, I/O on RA6
8. INTHS Internal Oscillator used as Microcontroller Clock Source, HS Oscillator used as USB Clock Source
9. INTIO Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, Digital I/O on RA6
10. INTCKO Internal Oscillator used as Microcontroller Clock Source, EC Oscillator used as USB Clock Source, FOSC/4 Output on RA6

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF
Capacitor values are for design guidance only. These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.** Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application. See the notes following this table for additional information.			
Crystals Used:			
4 MHz			
8 MHz			
20 MHz			

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM



17.0 UNIVERSAL SERIAL BUS (USB)

This section describes the details of the USB peripheral. Because of the very specific nature of the module, knowledge of USB is expected. Some high-level USB information is provided in **Section 17.10 "Overview of USB"** only for application design reference. Designers are encouraged to refer to the official specification published by the USB Implementers Forum (USB-IF) for the latest information. USB specification Revision 2.0 is the most current specification at the time of publication of this document.

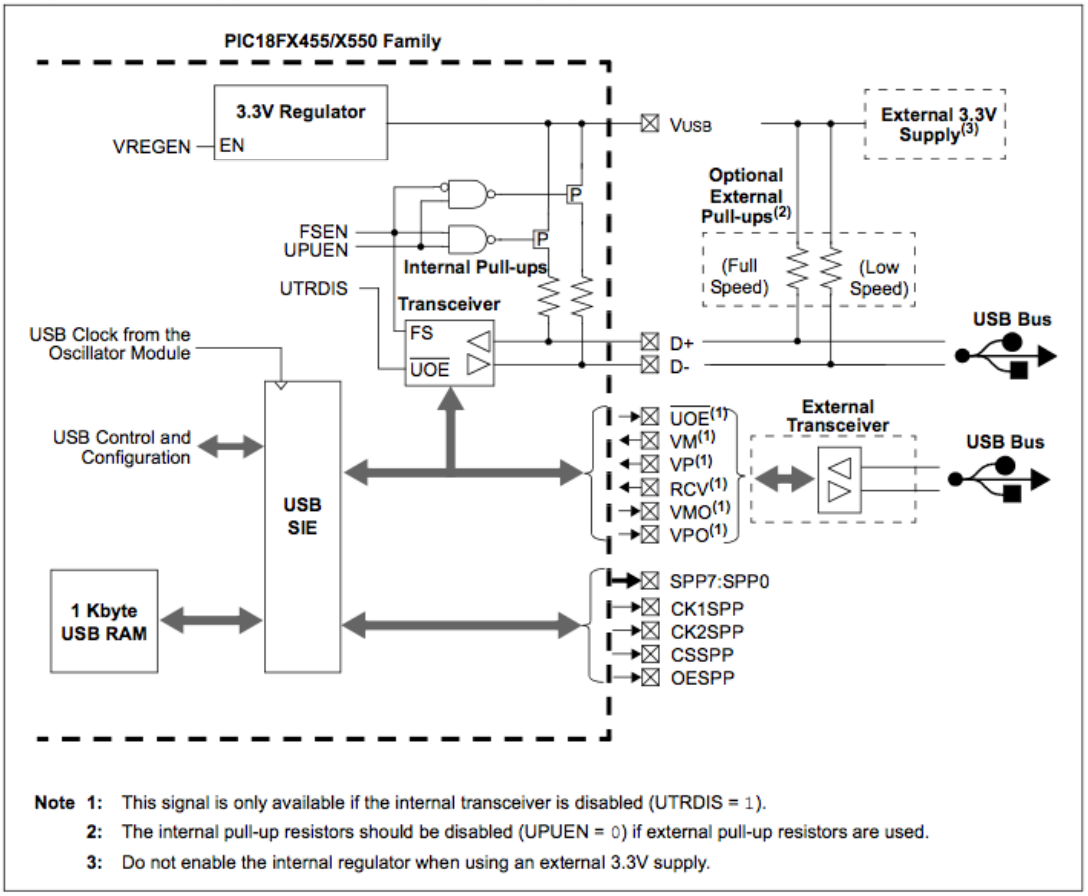
17.1 Overview of the USB Peripheral

The PIC18FX455/X550 device family contains a full-speed and low-speed compatible USB Serial Interface Engine (SIE) that allows fast communication between any USB host and the PIC® microcontroller. The SIE can be interfaced directly to the USB, utilizing the internal transceiver, or it can be connected through an external transceiver. An internal 3.3V regulator is also available to power the internal transceiver in 5V applications.

Some special hardware features have been included to improve performance. Dual port memory in the device's data memory space (USB RAM) has been supplied to share direct memory access between the microcontroller core and the SIE. Buffer descriptors are also provided, allowing users to freely program endpoint memory usage within the USB RAM space. A Streaming Parallel Port has been provided to support the uninterrupted transfer of large volumes of data, such as isochronous data, to external memory buffers.

Figure 17-1 presents a general overview of the USB peripheral and its features.

FIGURE 17-1: USB PERIPHERAL AND OPTIONS



Note 1: This signal is only available if the internal transceiver is disabled (UTRDIS = 1).

2: The internal pull-up resistors should be disabled (UPUEN = 0) if external pull-up resistors are used.

3: Do not enable the internal regulator when using an external 3.3V supply.

21.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 21-2, configures the functions of the port pins. The ADCON2 register, shown in Register 21-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 21-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Unimplemented(2)
1110 = Unimplemented(2)
1111 = Unimplemented(2)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D converter module is enabled
0 = A/D converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are available only on 40/44-pin devices.

REGISTER 21-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

21.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>) which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

21.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD (see parameter 130 in Table 28-29 for more information).

Table 21-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 21-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Assumes TAD Min. = 0.8 µs
Operation	**ADCS2:ADCS0**	**Maximum FOSC**
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	48.00 MHz
RC(2)	x11	1.00 MHz(1)

Note 1: The RC source has a typical TAD time of 2.5 µs.

2: For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead. Otherwise, the A/D accuracy may be out of specification.

28.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) **(Note 3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} **(Note 2)** ..... 0V to +13.25V
Total power dissipation **(Note 1)** 1.0W
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin ..... 250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 200 mA
Maximum current sourced by all ports ..... 200 mA

Note 1: Power dissipation is calculated as follows:
$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}/V_{PP}$/RE3 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}/V_{PP}$/RE3 pin, rather than pulling this pin directly to V_{SS}.

3: When the internal USB regulator is enabled or V_{USB} is powered externally, RC4 and RC5 are limited to -0.3V to (V_{USB} + 0.3V) with respect to V_{SS}.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.